IDEC Chip Design Contest

An Area-Effective and Low-Power Analog Spiking Neural Network Circuit with Current-Source Sharing Synapses and Coarse-Fine Comparing Neurons

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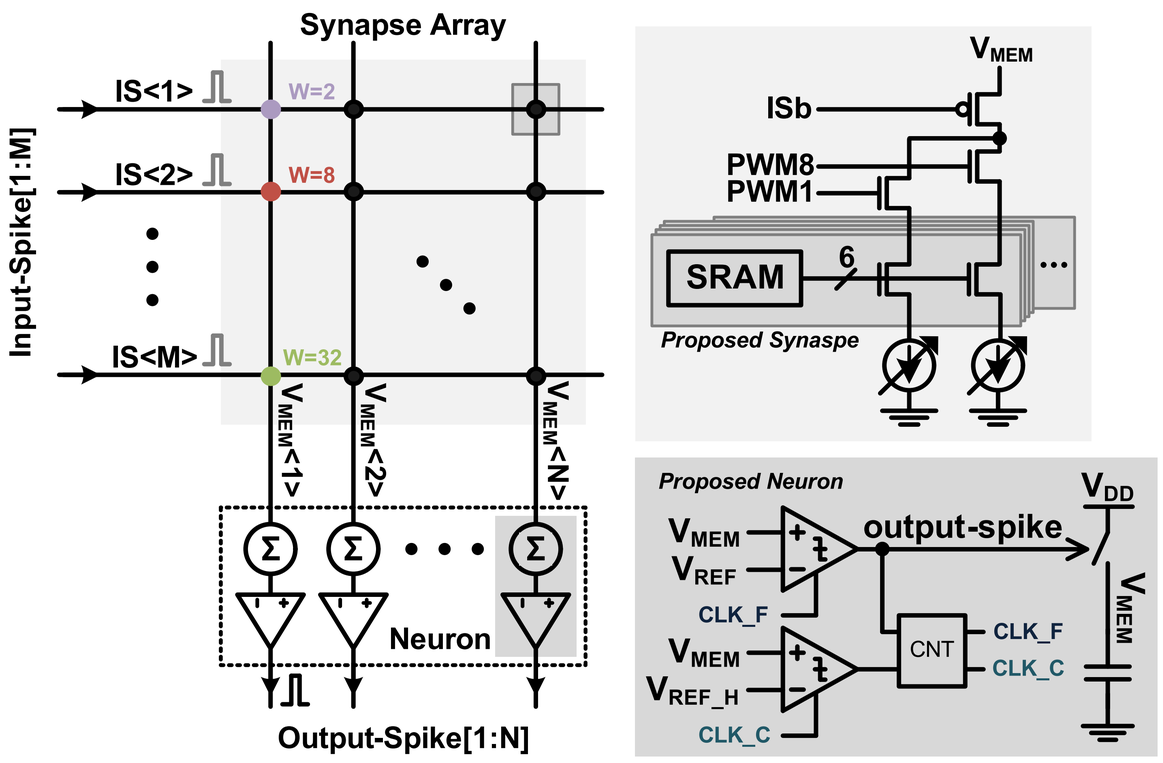
Introduction

This chip proposes an area-effective and low-power analog spiking neural network circuit with current-source sharing synapses and coarse-fine comparing neurons. The proposed synapse circuit divides the conventional synapse circuit into three blocks: current source, synapse switch, and global switch, and shares current source and global switch with 32 synapse switches to increase area efficiency. The proposed neuron circuit reduces neuron power by dividing the comparison section by adding a coarse comparator with less precision but low power consumption to the conventional fine comparator with high precision but high power consumption. The proposed analog SNN chip was fabricated using a 65nm CMOS process with VDD=1.2V. The current-source sharing synapse saves 60% synapse area. The Coarse-Fine comparing neuron dissipates 48.24μW/neuron, saves 43% neuron power.

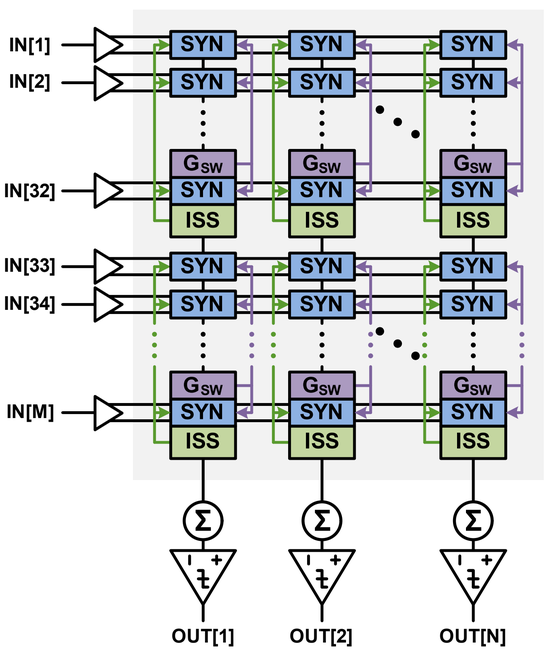
Architecture



Proposed analog spiking neural network model

This model consists of a low-area synapse circuit, a low-power neuron circuit, and SRAM memory. Each synapse stores a 6-bit weight through SRAM. The synapse uses the current DAC to generate a current proportional to the stored weight.

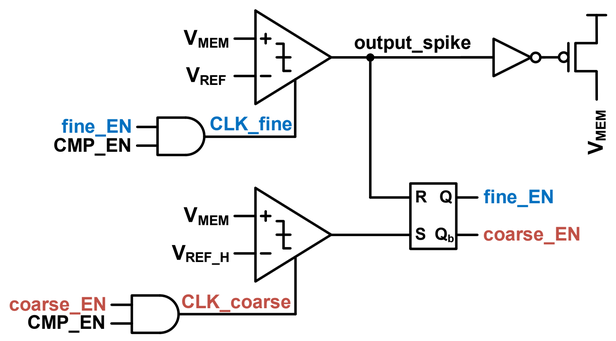
Synapse circuit

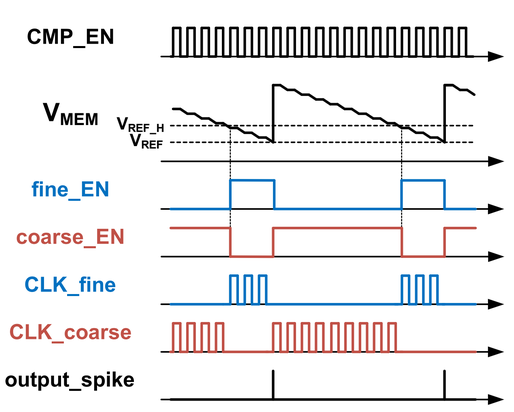


Proposed synapse circuit

The Synapse circuit divides the existing synaptic circuit into current sources, synaptic switches, and global switches, and shares 32 synaptic switches with current sources and global switches, increasing area efficiency.
The current source ISS was shared for every 32 SYN blocks, and the area of 32 synapses was reduced by 60%.

Neuron circuit

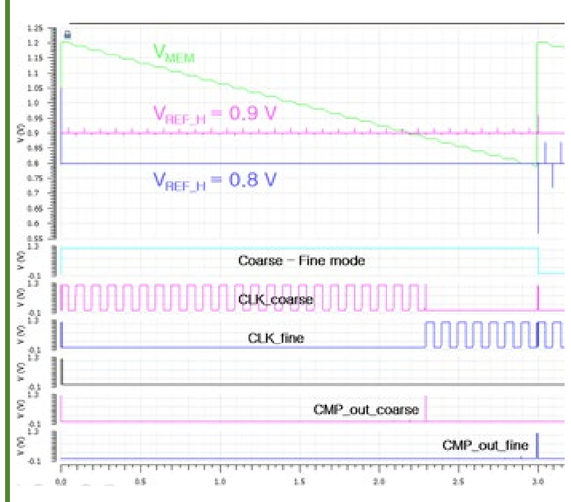




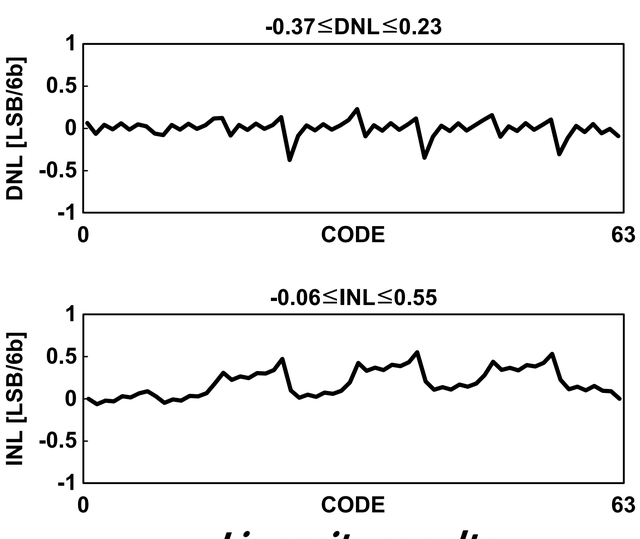
Proposed neuron circuit

The neuron circuit used a course-fine comparator to reduce power consumption.

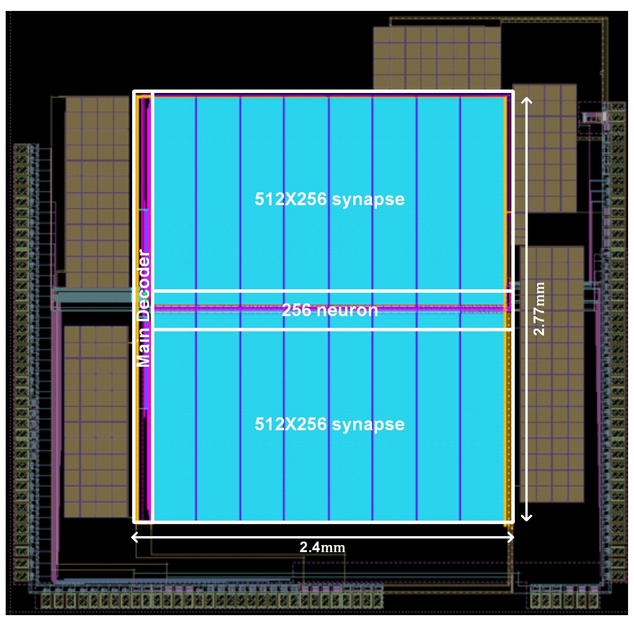
Results

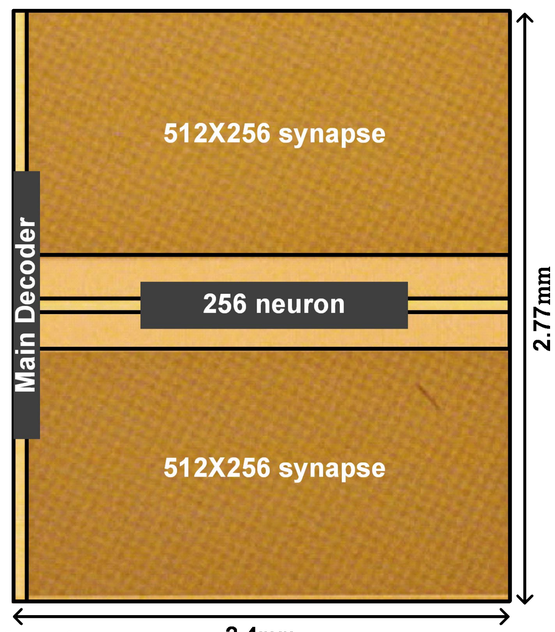


Simulation results



Linearity results





Chip layout & phothgraph

Conclusions

This chip proposes an area-effective and low-power analog spiking neural network circuit with current-source sharing synapses and coarse-fine comparing neurons. The proposed analog SNN chip was fabricated using a 65nm CMOS process with VDD=1.2V. The current-source sharing synapse saves 60% synapse area. The Coarse-Fine comparing neuron dissipates 48.24μW/neuron, saves 43% neuron power.

Acknowledgement

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